Remarks

The comments of the applicant below are each preceded by related comments of the examiner (in small, bold type).

2. Claim 13 is objected to because of the following informalities: the claim is missing a period at the end of the sentence. Appropriate correction is required.

Claim 13 has been amended.

3. Claim 52 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 49. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim 52 has been canceled.

5. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 contains the limitation "the input transfer register" on line 2. This limitation lacks sufficient antecedent basis. Appropriate correction is required.

Claim 7 depends on claim 58, which recites "an input transfer register".

7. Claims 13, 49, 52, 55, 56 and 61 are rejected under 35 U.S.C. 102(e) as being anticipated by Correale, Jr. et al. [US 6,587,905] (hereinafter "Correale").

Per claims 13, 49, 52, 55, 56 and 61, Correale teaches a data processor (see claim 4, "a data processing system", the processor is considered to be including the CPU, other Master devices, and the PLB Arbiter) comprising:

a plurality of programming engines (see Fig. 10, the Master devices);

a push arbiter (see Fig. 10, the PLB Arbiter) to arbitrate use of an unidirectional push bus (see Fig. 10, rdDBus) by a plurality of external memory resources that are external to the data processor (see Fig.10, the Slave devices), the push bus arbiter being internal to the data processor (see col. 4, lines 1-6, PLB and its arbiter are comprised within the processor architecture), the push bus to push data from the memory resources to an input transfer memory (not clearly shown by Correale in its drawings, but it is clear that a register must be present on a processor's input port which is connected to a data bus in a processor architecture, because processors can execute instructions and fetch data much faster than memories can be accessed to provide the data, and input/output registers are needed to synchronize the data transactions between a processor and a memory resource by using a system clock) associated with the programming engines; and

a pull bus arbiter (see Fig. 10, the PLB Arbiter) to arbitrate use of a unidirectional pull bus (see Fig. 10, wrDBus) by the external memory resources, the pull bus arbiter being internal to the data processor, the pull bus to pull data from an output transfer memory (not clearly shown by Correale, but it is clear that a register must be present on a processor's

output port which is connected to a data bus in a processor architecture, because processors can execute instructions and provide read/write data much faster than memories can be accessed to provide or store the data, and input/output registers are needed to synchronize the data transactions between a processor and a memory resource by using a clock) associated with the programming engines and to transfer the data to the memory resources.

Applicant disagrees. Correale does not disclose and would not have made obvious "a plurality of memory resources, each memory resource being associated with a memory controller," "a push bus arbiter to arbitrate use of the push bus by the memory resources," and "a pull bus arbiter to arbitrate use of the pull bus by the memory resources," as recited in claim 13, for at least two reasons.

First reason:

In claim 13, the push and pull bus arbiters arbitrate use of the push and pull buses by "memory resources" each being "associated with a memory controller." By contrast, Correale discloses "slave devices" but does not disclose or suggest that the slave devices include more than one memory resource each associated with a memory controller. Correale discloses an example that includes a slave memory controller 704 and a slave PCI bridge 705 (FIG. 7 and col. 5, lines 55-58). A slave PCT bridge is not a memory resource that is associated with a memory controller. Thus, Correale does not disclose or suggest the use of "a plurality of memory resources, each memory resource being associated with a memory controller," as recited in claim 13.

Second reason:

In claim 13, the push bus arbiter arbitrates "use of the push bus by the memory resources," and the pull bus arbiter arbitrates "use of the pull bus by the memory resources." This implies that more than one memory resource are attempting to use the push bus or pull bus, and the use of the push/pull bus by the memory resources is arbitrated by the arbiter. Because Correale discloses only one memory controller, there is no need to arbitrate use of the data buses by the single memory controller.

Moreover, the arbiter in Correale grants bus access to requesting master devices (col. 2, lines 29-30, col. 7, lines 14-15, col. 8, lines 21-22). The arbiter in Correale selects the highest

priority request and steers the given master's address and controls onto a bus to the slaves through a multiplexer (col. 4, lines 39-42). In Correale, the arbiter arbitrates requests from two or more masters. Correale does not disclose or suggest an arbiter that arbitrates requests from the slave devices. Thus, even if the Examiner contends that the "slave devices" in Correale correspond to the "memory resources" of claim 13, Correale does not disclose or suggest arbitrating use of the data buses by the memory resources as recited in claim 13.

Claims 49, 52, 55, 56, and 61 are patentable for at least similar reasons as those applied to claim 13.

> **9. Claims 1-7, 16-21, 26-29, 33-35, 37, 40, 41, 43-45, 50, 51, 53, 54 and 57-60 are rejected under U.S.C. 103(a) as being unpatentable over Correale and Shaylor [US 6,408,325] (hereinafter "Shaylor").**
>
> **Per claims 1, 26 and 37, it is clear the Correale already teaches most of the claims as described above (the programming agent in claim 56 is considered to be equivalent to the processing agent of claim 1), and further teaches issuing a write command (the pulling of data from the processing agent to the memory resources must be a result of a write command) and loading data into an output transfer memory of the processing agent (see the rejection of claims 13, 49, 52, 55, 56 and 61 above).**
>
> **Correale also discloses setting the output transfer memory to a read-only state, even though it does not explicitly recite this limitation. However, It should be clear that since processors can execute instructions and issue memory write request must faster than the actual write operations can be completed by accessing the much slower memory, the processor's output register must have its write enable control signal disabled while the data to be written to memory is ready to be transferred over the data bus, in order to avoid the data being overwritten by a new write data generated by the processor before the current transfer is complete.**
>
> **Correale does not teach executing a context. Shaylor teaches a multi-tasking and multi-threading processor that can enhance data processing efficiency (see Shaylor, col. 1, lines 46-50), the processor requires executing a context for each thread (see Shaylor, col. 1, lines 56-67). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to combine the teachings of Shaylor and Correale, in order to enhance data processing efficiency. As a result of the combination, Correale and Shaylor in combination teach "executing a context".**

Applicant disagrees. As discussed above, Correale does not disclose a plurality of memory resources, as recited in claim 1. Correale discloses a single slave memory controller 704 (FIG. 7 and col. 5, lines 55-58).

Moreover, although Correale discloses an arbiter that arbitrates write requests issued by master devices (col. 4, lines 38-45), Correale does not disclose "the memory resources obtaining access to the pull bus based on arbitration by the pull bus arbiter." In Correale, when a master

device issues a write command and gains access to a write bus after arbitration, the arbiter routes the addresses and write data to the slave devices (col. 4, lines 39-45). Correale does not disclose or suggest that the slave devices gain access to the write bus based on arbitration by the PLB arbiter.

Similarly, although Correale discloses an arbiter that arbitrates read requests issued by master devices (col. 4, lines 38-45), Correale does not disclose or suggest "the memory resources obtaining access to the push bus based on arbitration by the push bus arbiter," as recited in claim 1.

Claims 26 and 37 are patentable for at least similar reasons as those applied to claim 1.

All of the dependent claims are patentable for at least the same reasons as those applied to the claims on which they depend.

Any circumstance in which the applicant has addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner. Any circumstance in which the applicant has made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims. Any circumstance in which the applicant has amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: October 10, 2007

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